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Fixed negative interface charges compromise organic ferroelectric field-effect transistors

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ABSTRACT

Capacitance–voltage (*C–V*) and current–voltage measurements have been undertaken on metal-ferroelectric-semiconductor capacitors and ferroelectric field-effect transistors (FeFETs) using the ferroelectric polymer poly(vinylidenefluoride-trifluoroethylene) as the gate insulator and poly(3-hexylthiophene) as the active semiconductor. *C–V* measurements, voltage-dependence of gate currents and FeFET transfer characteristics all confirm that ferroelectric polarization is stable and only reverses when positive/negative coercive fields are exceeded for the first time. The apparent instability observed following the application of depletion voltages arises from the development of a negative interfacial charge which more than compensates the ferroelectric-induced shift, resulting in a permanent shift in threshold voltage to positive values. Application of successive bipolar voltage sweeps to a diode-connected FeFET show that significant remanent polarization is only induced in an *unpoled* device when the coercive field is exceeded during the first application of *accumulation* voltages. This initial polarization and its growth during subsequent bipolar voltage sweeps is accompanied by the accumulation of the fixed interfacial negative charges which cause the positive turn on voltages seen in *C–V* and transfer characteristics. The origin of the negative charge is ascribed either to layers of irreversible ferroelectric domains at the insulator surface or to the drift to the insulator-semiconductor interface of F^- ions produced electrolytically during the application of accumulation voltages.

1. Introduction

Organic electronic devices based on the metal–insulator-semiconductor (MIS) structure have been the focus of numerous studies in recent years [1–13]. Such devices operate on the same working principles as their inorganic predecessors i.e. those based on the ubiquitous and extensively studied [14–17] metal–oxide-semiconductor (MOS) class of devices which are at the heart of present-day integrated circuits. As is the case for MOS devices, the key processes occurring in MIS field effect transistors (FETs) such as accumulation/depletion behavior, charge transport and trapping, interface effects may all be studied using the simpler MIS capacitor structure [14–16]. For example, the transition from accumulation towards depletion, which occurs at the flatband voltage, V_{FB}, is readily observed as a decreasing capacitance in a capacitance–voltage (*C–V*) plot. Since organic FETs operate in accumulation, V_{FB} should, in principle, coincide with the turn-on voltage for the device but is dependent on a number of factors. These include interfacial charge trapping and polarization in the gate insulator which also may be studied using *C–V* measurements [14–16].

Controlled shifting of V_{FB} is the basis of operation of several different classes of non-volatile memory devices e.g. flash memory and the ferroelectric field-effect transistor

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(FeFET). In organic FeFETs, the gate insulator is formed from a ferroelectric polymer [3,18–21] whose polarization state is easily reversed electrically. Poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) appears to be a good candidate for such a remanently polarizable gate insulator. In these devices and depending on the direction of polarization in the ferroelectric, the active semiconductor layer is held either in the accumulation or depletion [21] mode, which define respectively the ON and OFF states of the device. Recent reviews [22,23] on organic electronics underline the potential of P(VDF-TrFE) based FeFETs for low cost memory applications. At present, performance parameters such as operating speed may not allow their application in high performance electronics but suggest utilization in low cost applications such as radio-frequency identification (RFID) tags.

Promising switching characteristics and retention times for P(VDF-TrFE) based FeFETs have been published by Gelinck [24] as well as by Naber et al. [20,22] and others [9,25,26]. They have reported switching times in the millisecond range and retention times of several hours, after which the ON state current deteriorated, leading to a concomitant decrease of the ON/OFF ratio by 30%. However, to be suitable for commercial applications, it is especially important that devices have long data retention times, ideally extending to several years.

Naber et al. [3,20,22] suggested that the lack of stable remanent depletion behavior in MIS capacitors and FeFETs utilizing P(VDF-TrFE) as the gate insulator and poly(3-hexylthiophene) (P3HT) as the active semiconductor, was caused by depolarization (relaxation) of the ferroelectric insulator upon reducing the depletion voltage. It was argued that to stabilize the ferroelectric polarization, compensating free electrons were required at the insulator/semiconductor interface which, it was argued, could not be supported by the p-type semiconductor P3HT. This argument ignores the evidence that the mechanism for polarization stabilization in P(VDF-TrFE) [27–32] requires injection into the insulator of charges which subsequently become trapped at the boundaries of the ferroelectric domains within the film. Hence, it is not necessary for interfacial negative charges to be provided by the semiconductor in order to obtain polarization stabilization. Negative charges can be injected into the P(VDF-TrFE) film through the gate contact and thereby stabilizing the polarization.

In an earlier publication [33], we reported the results of preliminary measurements which demonstrated that remanent polarization in P(VDF-TrFE)/P3HT MIS capacitors is indeed stable and only reverses when the coercive field is exceeded. We argued that the apparent loss of polarization was due to the *compensation* of the ferroelectric polarization by negative charges deeply trapped in the insulator at or near the semiconductor/insulator interface. Our results corroborated the findings of Ng et al. [34] in their detailed study of the long-term degradation of the memory effect in P(VDF-TrFE) FeFETs. These were important findings for understanding the apparent instability of organic FeFETs and necessitated further investigation. Based on the limited data available at the time, we surmised that these charges were electrons originating from the depleted semiconductor. Ng et al. [34] refer more generally to 'injected and subsequently trapped charges'.

In this paper we present more detailed results obtained both on MIS capacitors and FeFETs which confirm that the basic premise was correct viz. compensation by negative charges rather than a relaxation of the ferroelectric polarization. However, our new measurements, in particular the current–voltage characteristics of diode-configured FeFETs in forward and reverse bias, provide insights into the charge trapping process which indicate strongly that the negative charges originate from within the insulator itself.

2. Materials and methods

All devices were prepared in a class 1000 Clean Room by sequentially spin-coating a double layer of P(VDF-TrFE) (65/35 mol.%) from a 2-butanone solution onto a clean glass substrate furnished with evaporated Al electrodes. The semiconducting layer was spin-coated from a P3HT/chloroform solution after drying the P(VDF-TrFE) film at 120 °C for 12 h under vacuum to improve crystallinity. The devices were completed by vacuum-evaporating either top gold electrodes of area 10.2 mm^2 (capacitors) or gold source/drain interdigitated electrodes (FeFETs) with a source-drain gap $L = 100\ \mu m$ and an aspect ratio $W/L = 1485$. All devices were then annealed at 90 °C for 12 h under vacuum. Typical insulator and semiconductor layer thicknesses were 0.25 μm and 0.05–0.08 μm as measured on reference samples with a Dektak 3 ST surface profiler. Dielectric measurements were performed with the Novocontrol Alpha A impedance analyzer under a temperature controlled nitrogen atmosphere with bias voltages applied to the Al electrode. FETcharacteristics were measured under nitrogen using an Agilent 4155C Semiconductor Parameter Analyzer. In addition to obtaining transfer characteristics in the normal transistor configuration, measurements were also made on FETs configured as diodes (drain and gate connected together and grounded, see Fig. 1) and positive/negative voltages applied to the source electrode to forward/reverse bias the device.

3. MIS capacitance–voltage measurements

Several authors [35–38] have demonstrated that the effects of ferroelectric polarization can be separated from conduction processes in current–voltage (I–V) plots using the unipolar/bipolar voltage sweep regime illustrated in the inset of Fig. 2. If we ignore the conduction current and concentrate on displacement current effects, then the measured current density, J_m, flowing when the applied voltage is swept at a rate dV/dt is given by:

$$J_m = \frac{dQ}{dt} = C_i \frac{dV}{dt} + \frac{dP}{dt} \quad (1)$$

where dQ is the change in charge density on the electrodes, C_i the capacitance per unit area corresponding to the static dielectric constant of the ferroelectric layer and dP the incremental change in ferroelectric polarization occurring in time dt. In such measurements, the first term on the right hand side of Eq. (1) would superimpose a constant

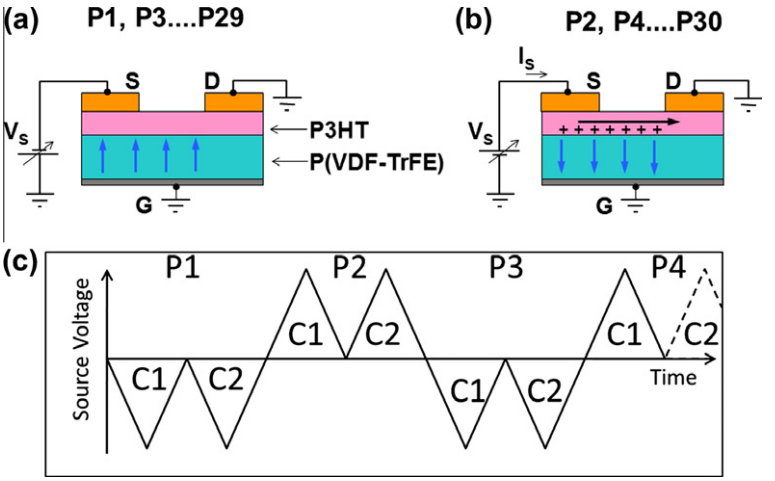

Fig. 1. Diode-configured FeFET in (a) reverse and (b) forward bias. The source voltage sequence used for measuring the output characteristics is shown in (c). Each bipolar cycle is labeled P1, P2, P3... with odd (P1, P3,...) and even (P2, P4,...) numbers corresponding to negative and positive source voltages respectively. For an ideal device in forward bias, ferroelectric polarization of the P(VDF-TrFE) should enhance charge carrier concentration in the accumulation channel but after switching direction in reverse bias should deplete the device even further.

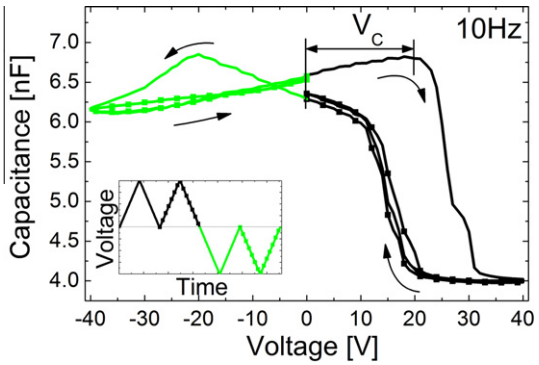

Fig. 2. Capacitance–voltage plots obtained for a MIS capacitor with a 0.25 μm thick insulator using the programmed voltage sequence shown in the inset and a probing frequency of 10 Hz.

displacement current on any conduction current present. If, however, during an initial voltage sweep the coercive field is exceeded and the ferroelectric polarization, P, reverses this will manifest itself as a peak in the I–V plot. If now a second unipolar sweep is undertaken P will remain unchanged and no peak will be observed, even when the coercive field is exceeded. Thus, if two unipolar voltage loops are applied to a ferroelectric, only the first will contain a contribution from the re-orientation of ferroelectric dipoles.

This approach is also applicable to C–V measurements since Eq. (1) is readily rewritten to yield C_m, the measured capacitance per unit area, i.e.

$$C_m = \frac{dQ}{dV} = C_i + \frac{dP}{dV} \tag{2}$$

where dP now represents the change in ferroelectric polarization occurring in the P(VDF-TrFE) film during an incremental change dV in the applied voltage. Consequently, a reversal in polarization will now manifest itself as a peak in the C-V plot. This behavior is clearly observed in the C–V plots in Fig. 2 which were obtained from our ferroelectric MIS capacitors using unipolar/bipolar voltage sweep cycles.

On the initial sweep to positive or negative voltages, the capacitance plots exhibit broad maxima. The return sweep and subsequent unipolar sweeps show only the underlying behavior expected of a MIS capacitor based on a p-type semiconductor i.e. essentially constant capacitance for accumulation voltages, $-V$, but decreasing to a lower constant value as the semiconductor becomes entirely depleted at positive values of V. Maxima in capacitance appear at approximately ± 20 V corresponding to the coercive field, $E_C \sim 60$ MV/m, of P(VDF-TrFE) [39]. Since capacitance maxima only occur on the first voltage sweep after polarity reversal, they must arise from the reversal of ferroelectric polarization in the insulator.

After polarization reversal during the positive voltage sweep, the device was expected to remain fully depleted until the subsequent negative voltage sweep had reached about −20 V when the polarization should reverse again. Instead, on the return voltage sweep, the capacitance rises and the device returns to accumulation at a low *positive* voltage. This behavior has been taken by some authors [3,19,20,22] as evidence that depletion occurs due to the collapse of ferroelectric polarization at positive bias. If this was the case, then a peak should be observed in the C–V plots in Fig. 2 during the second monopolar voltage sweep to positive bias: ferroelectric polarization should be re-established on exceeding the coercive field in the ferroelectric. This is clearly not the case and so it may be concluded that ferroelectric polarization is indeed stable even when the device is in depletion. The results presented here (Fig. 2) as well as in our earlier publication [33] confirm, therefore, that ferroelectric polarization is stable and only reverses when the coercive field is exceeded. We argued [33] that the narrower than expected hysteresis arose from an underlying shift in the flatband voltage of the device

caused by electrons drifting from the depleted semiconductor into trap states in the P(VDF-TrFE) at or near the interface with P3HT. This is similar to the report by Ledoyen et al. [26] which argued that the neutralization of the ferroelectric polarization in their P(VDF-TrFE)/p-silicon transistors was caused by interface and bulk trapping of electrons originating from the silicon inversion channel. Although our devices do not invert, nevertheless, this does not preclude the possibility that a low concentration of free electrons exist in the depletion region of our device and can drift to and become trapped in interface states. In our previous report [33] we estimated that, the effective interface density of trapped electrons required to compensate the effect of ferroelectric polarization *and* to produce a positive flatband voltage of 10 V was $\sim 3 \times 10^{13}$ cm^{-2}, a much greater density than in non-ferroelectric insulators [7].

Ledoyen et al. further showed that the rate of electron trapping was related to the oxygen concentration in the device ambient and to the porosity of the P(VDF-TrFE) layer [26]. Although our devices were vacuum-annealed at elevated temperatures and measurements made under nitrogen, this does not guarantee the complete removal of oxygen-related traps created during the device preparation stages undertaken in air. Therefore, it is conceivable, although less likely, that oxygen-related electron traps could also be present in our devices.

4. MIS admittance spectra

The phenomena giving rise to the effects seen in Fig. 2 can also be observed in the admittance spectra of these devices. Fig. 3 gives the frequency dependence of (a) capacitance and (b) loss (conductance/angular frequency) for a MIS-device with a 0.25 μm ferroelectric layer. Before the measurement, the device was poled several times by repeatedly switching the applied voltage between ±25 V. This procedure is necessary in order to achieve stable ferroelectric switching behavior in the P(VDF-TrFE) insulator [27,28] – a point we will return to later in Section 5. Frequency sweeps were subsequently undertaken by incrementing the bias voltage every 4 V from 0 V to 28 V and then decrementing at the same rate to 0 V. For clarity, only a sufficient number of plots are given in Fig. 3 to demonstrate the device response.The frequency response of an organic MIS capacitor of unit area is readily understood using the equivalent circuit model in Fig. 4 in which $C_i = \varepsilon_i\varepsilon_0/d_i$ and R_i represent an insulator of thickness d_i and relative permittivity ε_i with ε_0 the permittivity of free space, $C_d = \varepsilon_s\varepsilon_0/d_p$ and R_d a depletion region of width d_p and relative permittivity ε_s, $C_b' = \varepsilon_s\varepsilon_0/(d_s - d_p)$ and $R_b' = \rho_s(d_s - d_p)$ the semiconductor layer of resistivity ρ_s and initial width d_s. Except at the highest frequencies, the effect of the contact resistance, R_{el}, is negligible while the resistances R_i and R_d are normally sufficiently high to be ignored. The measured admittance, Y, of this circuit can then be considered as a capacitance C_P in parallel with a conductance G_P and given by:[6,7]

$$Y = G_P + j\omega C_P = \frac{-\omega^2 C' C_b' R_b' + j\omega C'}{1 + j\omega R_b'(C' + C_b')} \tag{3}$$

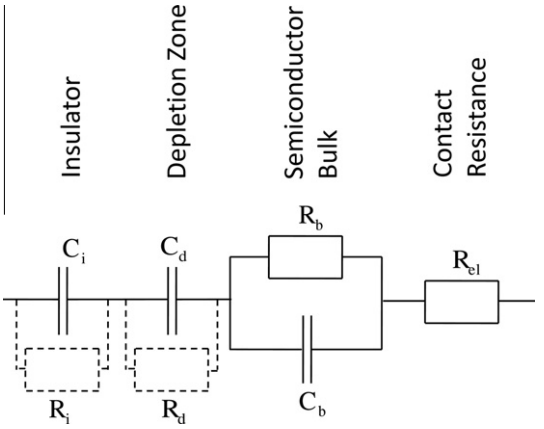

Fig. 3. Equivalent circuit of a MIS diode of unit area. C_i, C_d and C_b represent the capacitances of the insulator, depletion layer and bulk semiconductor respectively while R_i, R_d, R_b and R_{el} represent respectively the leakage resistance of the insulator and depletion region, the conductivity of the bulk semiconductor and any series resistance associated with the electrodes.

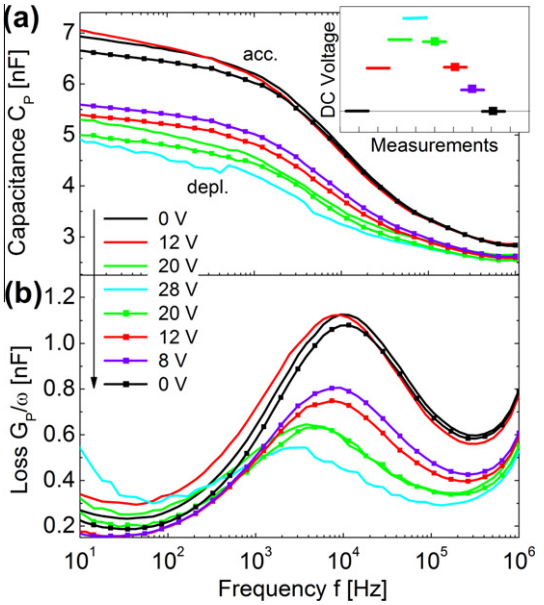

Fig. 4. Capacitance (a) and loss (b) spectra of a MIS capacitor with a 0.25 μm thick insulator. For each frequency sweep, the voltage was incremented in 4 V steps from 0 V to 28 V and then reduced again to 0 V. The sequence of dc voltages applied is given in the legend but for clarity only a few plots are shown.

with

$$C_P = C_g + \frac{C' - C_g}{1 + \omega^2 R_b'^2 (C' + C_b')^2} \tag{4}$$

and

$$\frac{G_P}{\omega} = \frac{\omega R_b' C'^2}{1 + \omega^2 R_b'^2 (C' + C_b')^2}. \tag{5}$$

In these equations, ω is the angular frequency, C' the series sum of C_i and C_d, and C_g the series sum of C' and C'_b. The characteristic relaxation time of this circuit is given by $R'_b(C' + C'_b)$ and since C', C'_b and R'_b change with voltage as the depletion region expands through the semiconductor, then its relaxation frequency, f_R, which is related to the mobility of charge carriers in the bulk semiconductor layer, will increase through the range

$$\frac{1}{2\pi R_b(C_i + C_b)} \leq f_R \leq \frac{1}{2\pi\rho_s\varepsilon_s\varepsilon_0} \quad (6)$$

as the device is driven from accumulation to full depletion [6].

Based on the equivalent circuit description above, the results in Fig. 3 are readily explained. As can be seen, the low frequency capacitance remained at ~6.5 nF for applied voltages up to 12 V which is consistent with the device in accumulation i.e. dominated by the insulator capacitance C_i owing to the relatively low value of R_b compared with R_i. In the thinner P(VDF-TrFE) layer in this device, the coercive field was attained with an applied voltage greater than ~12 V when the P3HT was eventually driven into depletion causing the low frequency capacitance to decrease as the depletion region expanded, in keeping with Eq. (4). Voltages in excess of 30 V and, therefore, close to breakdown would have been required to completely deplete the device i.e. to reduce the low frequency capacitance to its high frequency value (~2.5 nF) corresponding to the series sum of the insulator and semiconductor capacitances [6].

On reducing the applied voltage below 8 V, the low frequency capacitance began to grow again to its accumulation value, reflecting the neutralization of the ferroelectric polarization observed in Fig. 2.

The main feature in the loss spectra in Fig. 3(b) is the mid-frequency maximum predicted by Eq. (5) and arising from the Maxwell–Wagner response of a two-layer dielectric capacitor [6,40]. When the device is in accumulation, the loss maximum is essentially constant and independent of applied voltage. Thus, the left hand limit of Eq. (6) applies from which we may estimate R_b since f_R = 10 kHz, $C_i = 6.8 \times 10^{-9}/10.2\text{x}10^{-6} = 6.64 \times 10^{-4}$ F/m^2 and $C_b = 4.11 \times 10^{-4}$ F/m^2 (estimated by assuming the high frequency capacitance, 2.6 nF is the series sum of the insulator and semiconductor capacitances). Thus R_b = 0.0148 Ωm^2 and by assuming that the p-type doping density in vacuum-annealed P3HT is typically 1×10^{22} m^{-3} [6,40], ε_s = 3 and the film thickness is ~50 nm, we deduce that the bulk mobility is $\sim 2 \times 10^{-5}$ cm^2/Vs which is at the lower end of the range given in [6].

As predicted by Eq. (5), the maximum loss decreases when ferroelectric switching at the coercive field causes the device to deplete. When fully depleted, the right hand limit of Eq. (6) applies and since $\rho_s\varepsilon_s\varepsilon_0 = R_bC_b$, f_R was expected to increase only slightly to 26 kHz. As discussed above, though, the device only partially depletes (Fig. 4(a)) so the shift to higher frequency is expected to be minimal. However, the maximum loss shifts to *lower* frequencies as the depletion deepens. Presumably, other factors are important. For example, Torres and Taylor [6] attributed a similar observation to the decrease of order within the P3HT film on moving away from the interface [41,42] resulting in a reduced mobility and higher resistivity. The lower value for mobility estimated above is certainly indicative of greater disorder in our films compared to those investigated in [6] but compare well with mobilities found in P3HT fractions of lower molecular weight, which are known to show a twisted and disordered chain conformation [42–45].

The admittance measurements reflect, therefore, the behavior in the *C*–*V* plots in Fig. 3. On incrementing from negative to positive voltages, ferroelectric polarization maintains the device in accumulation until the coercive field is reached at ~15 V when reversal of the polarization causes the device to deplete. Further increases in voltage simply lead to deeper depletion in the MIS capacitor which is reflected in the decreasing magnitudes of the low-frequency capacitance and loss peak maximum. The early onset of accumulation when the voltage is reduced, in this case just below 8 V, is consistent with observations in the *C*–*V* plots in Fig. 3.

5. FeFET characteristics

The *C*–*V* measurements reported in Section 3, supported by the admittance spectra in Section 4, provide clear evidence that the transition from accumulation to depletion in the MIS capacitor is induced by the reversal of ferroelectric polarization at a sufficiently high positive voltage. The results in Section 3 clearly demonstrate that the reverse transition i.e. from depletion to accumulation is governed by a flatband voltage shift arising from the trapping of an effective negative charge at the interface. Consequently, this transition now occurs at low positive voltages rather than at a negative voltage (−15 to −20 V) corresponding to the coercive field required for restoration of the original polarization direction. In this section, we investigate how these same effects influence transistor performance.

5.1. Transfer characteristics

Fig. 5(a) gives the transfer characteristics i.e. plots of source current vs gate voltage (I_S–V_G) for drain voltages, V_D, set to 0 V and −5 V. The gate current, I_G, recorded simultaneously is plotted in Fig. 5(b). The current maxima in I_G occur only when $|V_G|$ corresponds to the coercive field [34,46] and provide clear evidence for polarization reversal, as discussed in Section 3 and described by Eq. (1). Applying a drain voltage of −5 V caused the current maxima to shift by −5 V compared to the case for V_D = 0 V. This is not surprising since a negative drain voltage will enhance the electric field experienced by the insulator near the drain when the device is in depletion but will reduce the field when in accumulation. Shoulders on the positive voltage side of the peaks coincide with the V_D = 0 V case confirming that reversal of ferroelectric polarization also occurs under the source electrode and presumably then, under the whole of the channel with the relative contributions proportional to the respective overlap areas with the gate electrode.

In keeping with the *C*–*V* measurements, when V_G is swept from −40 V to +40 V, initially I_S falls slowly but

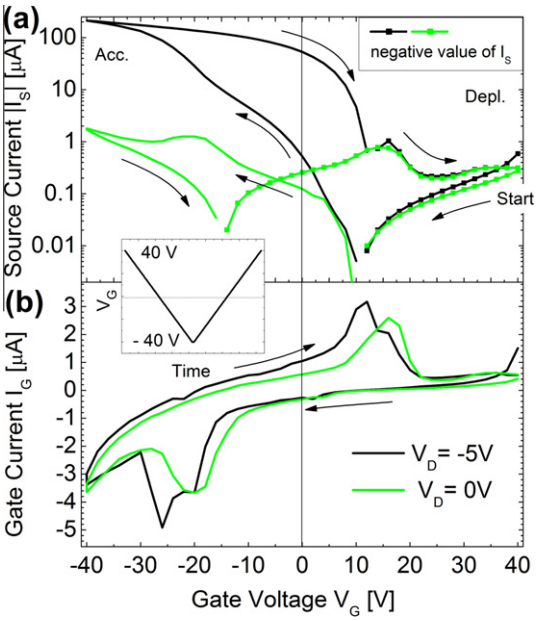

Fig. 5. (a) Transfer (I_S–V_G) characteristics obtained for $V_D = 0$ V and $V_D = -5$ V and with the source grounded in both cases. (b) The corresponding dependence of gate current, I_G, on gate voltage, V_G, obtained using the bipolar voltage cycle depicted in the inset. Negative values of I_S are marked with the symbol (-■-).

when the coercive field is exceeded at ~10 V, ferroelectric polarization reverses and I_S decreases rapidly as the device is driven into depletion. Above 12 V, I_S changes sign but remains low.

In this range, I_S is essentially the mirror image of I_G and almost indistinguishable from the plot for $V_D = 0$ V, confirming that the channel current is negligible. In the range from 5 V to −15 V, I_S increases well above I_G heralding the establishment of an accumulation channel even before the coercive field is reached. This is similar to the results reported recently by Asadi et al. [46] In this latter case, I_D increased above I_G as V_G was swept between +25 V and −25 V with a further increase observed when the coercive field was reached at about −70 V – their devices incorporated a much thicker (1.3–1.4 μm) ferroelectric layer than ours. It should be noted here that for the same effective density of interface trapped charge the shift in flatband voltage, and hence turn-on voltage, will be directly proportional to the insulator thickness suggesting similar levels of negative charge trapping in our devices as in those of Asadi et al.

While the above results are consistent with our *C*–*V* plots, which similarly showed the device accumulating for positive values of V_G, once in accumulation the *C*–*V* plot is not sensitive to the *degree* of accumulation. This is not the case in the transfer characteristic, where reversal of the ferroelectric polarization between −15 V and −30 V in the accumulation regime clearly caused a further order of magnitude increase in I_S which reached ~200 μA when $V_G = -40$ V. Again this is similar to the observations of Asadi et al. [46].

Despite the early onset of accumulation there is, nevertheless, a two orders of magnitude difference in the measured I_S for $V_G = 0$ V which is significantly greater than the ratio of ~40 observed by Ng et al. [34] Taken together with the width of the hysteresis loop in Fig. 5(a) this difference is sufficiently large for one-transistor (1T) digital memory applications, with the particular advantage here that operating voltages are low.

5.2. Diode-configured FeFET

We have also investigated the performance of our FeFET in the diode configuration (gate and drain connected as shown in Fig. 1). As will be seen below, this configuration is useful for investigating ferroelectric polarization and associated processes occurring at the interface. In particular, evidence is provided to support our contention above that ferroelectric polarization is stable but is compensated by the accumulation of negative interfacial charge.

Again we apply the unipolar/bipolar voltage cycles depicted in Fig. 1(c) but this time to the source contact. We focus here, though, on the evolution of the source current vs. source voltage (I_S–V_S) characteristic of the diode-configured FeFET in response to successive negative/positive poling cycles P1, P2, P3…P30. In Fig. 6(a) are shown the two unipolar cycles (C1,C2) corresponding to the negative poling cycles P1, P3, P5 and P29. Similarly in Fig. 7(a) are shown cycles C1,C2 corresponding to the positive poling cycles P2, P10 and P30 which were obtained after the negative poling cycles P1, P9 and P29, respectively.

With the gate and drain grounded, the diode-configured FeFET is normally in forward/reverse bias for positive/negative V_S. In this configuration the device current, I_S, is given by:[14]

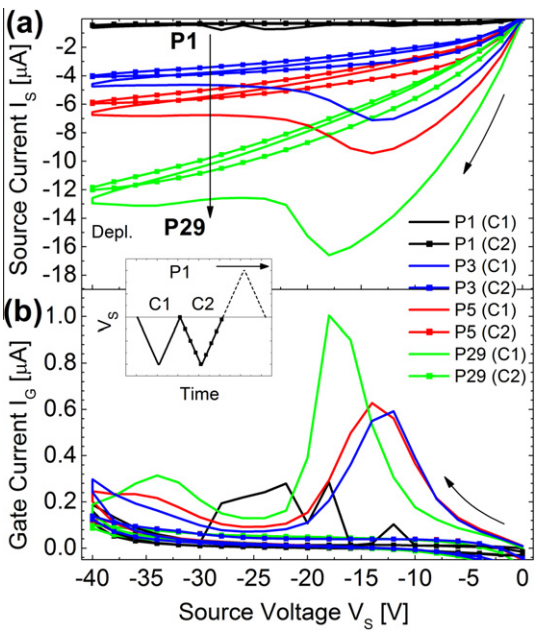

Fig. 6. (a) I_S–V_S characteristics for negative voltages applied to the source of a diode-configured FeFET. (b) The associated gate currents, I_G, all obtained using the source voltage pattern given in Fig. 1(c). As indicated in the inset, the plots correspond to the two uni-polar cycles, C1 and C2, and for clarity are given for poling cycles P1, P3, P5 and P29 only.

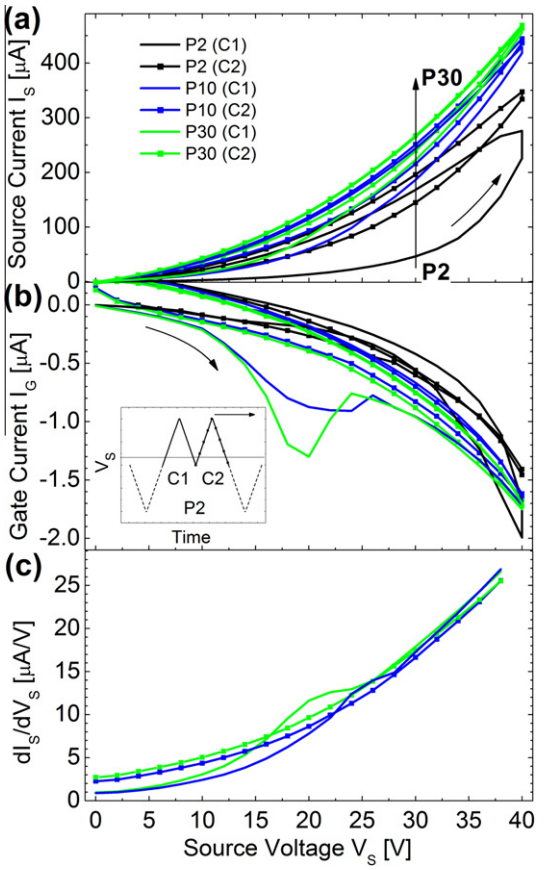

Fig. 7. (a) I_S–V_S characteristics for positive voltages applied to the source of a diode-configured FeFET and (b) the associated gate currents, I_G, all obtained using the source voltage pattern given in Fig. 1(c). As indicated in the inset, the plots correspond to the two uni-polar cycles, C1 and C2, and for clarity are given for poling cycles P2, P10 and P30 only. In (c) are plots of dI_S/dV_S vs V_S for the forward sweeps of C1 and C2 corresponding to poling cycles P10 and P30.

$$I_S = \frac{W}{2L}\mu C_i\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right] \tag{7}$$

where μ is the carrier mobility in the accumulation channel, V_T the threshold voltage and $V_G = V_D = -V_S$ so that

$$I_S = K\left(\frac{1}{2}V_S^2 + V_T V_S\right) \tag{8}$$

where $K = W\mu C_i/2L$. For positive V_S, I_S should increase monotonically, albeit superlinearly, with increasing V_S. (For negative values of V_T the device will only turn on when the term in brackets is positive). For negative V_S, the drain electrode now acts as the hole injecting contact and a *p*-channel device would normally be turned off. Hole currents can only flow for positive values of V_T in which case a typical output characteristic should be observed i.e. $|I_S|$ initially increasing linearly with increasing $|V_S|$ before eventually saturating above pinch-off.

In our FeFETs, this ideal behavior will be modified by any changes in V_T which occur when the ferroelectric polarization is reversed. The current maxima in the I_G–V_S plots in Figs. 6(b) and 7(b) provide clear evidence (c.f. Eq. (1)) for these transitions [34] which are seen also to correlate with departures of $|I_S|$ from the ideal behavior in Figs. 6(a) and 7(a).

Of interest initially, though, is the *growth* of the ferroelectric polarization in successive poling cycles as evidenced by the growth in the gate current maxima to ~1 μA (Figs. 6(b) and 7(b)), which in turn manifests itself as increases in $|I_S|$ for both voltage polarities.

During the first poling cycle P1, when *negative* voltages are applied to the source of the unpoled device (Fig. 6(a)), $|I_S|$ remains low (<0.5 μA) over the whole voltage range as would be expected for a diode-configured FET biased into depletion. However, the device becomes more conductive in successive poling cycles with the maximum in current for negative V_S eventually saturating at ~16 μA during the C1 cycle for voltage sweeps P25-P29. In each C1 cycle, when the coercive field is exceeded, the device attempts to turn off. However, the current only decreases by ~2–3 μA, thereafter remaining constant. On the return sweep to 0 V, $|I_S|$ decreases monotonically to zero in a manner similar to a conventional output characteristic. The I_S–V_S plots obtained during C2, the second unipolar cycle, are similar to those obtained on the return sweep, albeit slightly lower.

A possible explanation for elevated currents at negative V_S is that *n*-channel behavior has been induced. Although ambipolar conduction has been demonstrated in specially prepared P3HT FETs [47], an electron accumulation channel is not formed in our device as evidenced by the transfer characteristic in Fig. 5(a). Rather, the drain is now acting as the hole source with an accumulation channel being maintained by positive values of V_T. When the remanent polarization reverses, V_T simply decreases in value rather than reverse sign owing to the presence of a negative fixed interface charge.

When positive voltages are applied to the source during the even-numbered poling cycles P2, P4…P30, the resulting superlinear characteristics in Fig. 7(a) are in accord with Eq. (7). When the coercive field is reached at voltages in the range 15 V < V_S < 25 V, the remanent polarization reverses thereby attracting additional holes into the accumulation channel as depicted in Fig. 1(b). This should lead to step changes in I_S during the forward sweep of the C1 cycles. However, for positive V_S, the transitions in I_S are not as well-defined as in Fig. 6(a) and are best identified in the differential plot, dI_S/dV_S vs V_S (Fig. 7(c)).

From Eq. (8) and for positive V_S

$$\frac{dI_S}{dV_S} = K(V_S + V_T) \tag{9}$$

suggesting that the plots in Fig. 7(c) should increase linearly with a gradient proportional to the carrier mobility through the constant K. If V_T becomes more positive when the coercive field is exceeded, this should lead to a step increase in I_S. The underlying trends in Fig. 7(c) are clearly not linear, presumably reflecting the superlinear dependence of carrier mobility on gate voltage [48] arising from trap modulation of carrier transport in the accumulation channel. Nevertheless, for polarization cycles P10 and P30, the presence of transitions in the range 15 V < V_S < 30 V in the forward sweep of C1 is clearly evi-

dent, but were absent in the reverse sweep and, as seen in Fig. 7(c), in the corresponding C2 cycle.

The noisy gate current in cycle C1 of P1 (Fig. 6(b)) suggests that some domain alignment may be occurring during the first application of depletion voltages to a new device. However, there is no evidence for polarization reversal in cycle C1 of P2 in Fig. 7(b), confirming that little or no remanent polarization was induced by the two preceding unipolar sweeps to −40 V. Rather, sufficient ferroelectric alignment leading to significant remanent polarization was only induced during the *first* excursion to high *accumulation* voltages. Only then did a clear signature for polarization reversal appear in the subsequent sweep to negative voltages (see P3, C1 in Fig 6(a)). Further bipolar voltage cycles simply increased the degree of domain alignment until saturation was reached.

This growth of polarization in ferroelectric polymers during successive voltage reversals has been observed by others. The phenomenon was reported by Guy and Unsworth [49] for PVDF and attributed to conformational transition of the crystal structure from Form II (α-PVDF) to Form I (β-PVDF). On the other hand, based on their studies of P(VDF-TrFE), Reynolds et al. [50] concluded that the growth of polarization arose from improved alignment of ferroelectric domains by the electric field. Based on this latter model, voltage-cycling can then be viewed as a means of 'annealing' out the defects which hinder the alignment of polar groups in the ferroelectric domains. Eberle et al. [27–29] further showed that the growth of remanent polarization in P(VDF-TrFE) films depended on both the magnitude of the applied electric field and the poling time. Only at very high fields (160 MV/m), higher than reached here, was full polarization obtained in a single poling step. Application of a lower field, 120 MV/m, led to a slower rise in polarization and to a lower remanent polarization. Importantly for our devices, they and others [9,32,51–54] have also shown that bipolar charge injection from the electrodes is essential for establishing a high, stable, remanent polarization. These injected charges migrate to the surfaces of the ferroelectric domains not only at the film surface but also in the bulk [31].

It is not surprising, therefore, that accumulation voltages which provide the conditions for facile double injection into the insulator, are required to stabilize ferroelectric alignment. The rapid rise in both I_G and I_S for $V_S > 30$ V during the first accumulation voltage cycle P2(C1) and the subsequent hysteresis exhibited by I_S are all indicators of the onset of ferroelectric alignment. For all subsequent uni/bipolar voltage cycles, the device remains in accumulation; polarization reversal simply changing the degree of accumulation. Interestingly, as the degree of ferroelectric alignment grows, polarization reversal appears to become easier (occurs at lower voltages) for positive V_S but more difficult for negative V_S, presumably reflecting the positive shift in V_T.

For the device to maintain a conducting channel for all cycles after P2, suggests that domain alignment during the first positive voltage sweep must have been accompanied by the appearance of fixed negative charge in the insulator at, or close to, the insulator/semiconductor interface. Two sources of such a charge are possible:

(a) The ferroelectric polarization may not be completely reversible. For example, Eberle et al. [28] suggest that after several polarity reversals, the ferroelectric domains adjacent to the insulator surfaces become stable; only those more central domains away from the surfaces can reverse their polarization. However, it is not clear that such 'layering' of the polarization could occur in the much thinner films used here.

(b) Injected negative charges could become trapped at the insulator/semiconductor interface. In our previous publication [33] based on limited preliminary information, we suggested that electrons were injected from the P3HT into the insulator when the structure was biased to full depletion. The evidence in Figs. 6 and 7, suggests otherwise, that any negative charges must be introduced during the application of accumulation voltages and must originate, therefore, at the gate electrode and drift to the insulator/semiconductor interface. This is certainly consistent with the higher gate currents observed for positive V_S.

Bihler et al. [53,54] presented strong evidence that the application of a poling field to a PVDF film caused an electrochemical reaction leading to the dissociation of F^- and H^+ ions from the PVDF polymer chain. These ions then contributed not only to the conduction process in the polymer but also stabilized the ferroelectric domains. Some of these ions even recombine leading to detectable quantities of HF gas during the poling procedure [28,29,53,54]. It is feasible then that some fraction of the F^- ions drift through the insulator to become trapped at the interface. Free ions in the insulator would also lead to the gradual upward/downward drift of I_S observed during the two unipolar cycles when positive/negative source voltages were applied and may contribute to the long-term degradation of the polarization observed by Ng et al. [34].

This compensation of ferroelectric polarization by free charges in the insulator has implications for the further development of memory devices based on P(VDF-TrFE). Since injected charges are essential for stabilizing the ferroelectric domains [9,44,51,52,54], any measures taken to prevent charge injection completely would lead also to the loss of the ferroelectric properties of the insulator.

In order to improve device performance in terms of retention time, width of hysteresis and ON/OFF ratio further investigations are required which focus on (a) charge injection from the gate electrode, (b) charge migration through the insulator and (c) the charge trapping mechanism at the insulator/semiconductor interface. Charge injection studies should identify the injection mechanism with a view to reducing direct electron injection and/or electrolytic production of F^-. Both processes will be strongly influenced by the electrode material. Combining our measurements on the diode-configured FeFET with the published literature suggests strongly that F^- ions may be drifting through the insulator. By suppressing this migration, fewer charges will reach the interface. Possible options for achieving this include optimizing P(VDF-TrFE) film preparation, using blends incorporating polymers such as poly(methyl methacrylate) (PMMA) or using different mole-fractions of TrFE. Identifying the nature of the

negative interface charges using various surface analytical techniques incuding secondary ion mass spectrometry is particularly important. Thereafter, the concentration of such sites may be reduced by carefully designed surface treatments.

6. Conclusion

The *C–V* plots and admittance spectra obtained from MIS capacitors formed from the ferroelectric polymer P(VDF-TrFE) as the insulator and P3HT as the active semiconductor both confirm our previous findings. Once established after several bipolar voltage cycles, ferroelectric polarization in P(VDF-TrFE) is stable as evidenced by the capacitance maxima in Fig. 2 and the gate current maxima in Figs 5–7. From the admittance spectra in Fig. 3 we deduced that the hole mobility in the bulk P3HT was $\sim 2 \times 10^{-5}$ cm^2/Vs and, therefore, at the lower end of previously reported values. Our *C–V* measurements confirm unambiguously that switching at the coercive field is responsible for the transition from accumulation to depletion but that the return transition from depletion to accumulation is governed by deeply trapped negative charge at the interface or in the bulk insulator.

The transfer characteristics of a FeFET formed from the same materials show that trapped negative charge induces significant accumulation even when the ferroelectric polarization should be maintaining the device in an off state. However, the device current did increase by a further order of magnitude once the coercive field was exceeded and the polarization reversed. Despite the reduced hysteresis caused by the early accumulation, P(PVDF-TrFE) devices can still be operated at low voltages with an ON/OFF ratio that is sufficiently large for one-transistor (1T) digital memory applications, thus confirming the potential of PVDF and its copolymers for nonvolatile memory applications.

The most interesting results were obtained from the diode-configured FeFET. These showed that significant remanent polarization was only achieved when the device was biased for the first time into accumulation, a condition allowing double injection into the insulator. In successive bipolar voltage cycles, the device current grew rapidly, reflecting the growth of ferroelectric polarization and an associated fixed interfacial negative charge. The ferroelectric polarization gave rise to reversible shifts in V_T at positive and negative coercive fields which were smaller than the permanent positive shift in V_T caused by the fixed negative charge. Drawing on the comprehensive studies of the ferroelectric state in P(VDF-TrFE) reported in the literature, the negative fixed charge could arise from irreversible ferroelectric domains in surface layers or, more probably, from the electrolytic dissociation of P(VDF-TrFE) molecules at the gate electrode to create F^- ions which drift to the insulator/semiconductor interface.

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References

[1] A. Tsumura, H. Koezuka, T. Ando, Appl. Phys. Lett. 49 (1986) 1210.
[2] R. Naber, M. Mulder, B. de Boer, P. Blom, D. de Leeuw, Organic Electron. 7 (2006) 132.
[3] R. Naber, J. Massolt, M. Spijkman, K. Asadi, P. Blom, Appl. Phys. Lett. 90 (2007) 113509.
[4] E. Meijer, C. Tanase, P. Blom, E. van Veenendaal, B.-H. Huisman, D. de Leeuw, T. Klapwijk, Appl. Phys. Lett. 80 (2002) 803838.
[5] D.M. Taylor, J.A. Drysdale, I. Torres, O. Fernández, Appl. Phys. Lett. 89 (2006) 183512.
[6] I. Torres, D.M. Taylor, J. Appl. Phys. 98 (2005) 073710.
[7] N. Alves, D.M. Taylor, Appl. Phys. Lett. 92 (2008) 103312.
[8] D.M. Taylor, IEEE Trans. Dielectr. Electr. Insul. 13 (2006) 1063.
[9] S. Lim, A. Rastogi, S. Desu, J. Appl. Phys. 96 (2004) 5673.
[10] M. Estrada, I. Mejia, A. Cerdeira, B. Iñiguez, Solid State Electron. 52 (2008) 53.
[11] J.H. Burroughes, C.A. Jones, R.H. Friend, Nature 335 (1988) 137.
[12] P. Stallinga, H.L. Gomes, Organic Electron. 7 (2006) 592.
[13] Z. Bao, J. Locklin, Field Effect Transistors, CRC Press, Boca Raton, 2007. 103f.
[14] S. Sze, Physics of Semiconductor Devices, third ed., Wiley–Interscience, New York, 2007 (p. 297f).
[15] E. Nicollian, A. Goetzberger, Bell Sys. Tech. J. 46 (1967) 1055.
[16] E. Nicollian, J. Brews, MOS Physics, Technology, Wiley–Interscience, 1982 (p. 423f).
[17] S. Miller, P. McWhorter, J. Appl. Phys. 72 (1992) 5999.
[18] S.-W. Jung, S.-M. Yoon, S.-Y. Kang, K.-J. Choi, W.-C. Shin, B.-G. Yu, Electrochem. Solid State Lett. 12 (2009) H325.
[19] R. Naber, P. Blom, Appl. Phys. Lett. 85 (2004) 2032.
[20] R. Naber, B. de Boer, P. Blom, D. de Leeuw, Appl. Phys. Lett. 87 (2005) 203509.
[21] T. Reece, S. Ducharme, J. Appl. Phys. 106 (2009) 124505.
[22] R. Naber, K. Asadi, P. Blom, D. de Leeuw, B. de Boer, Adv. Mater. 22 (2010) 933.
[23] P. Heremans, G. Gelinck, R. Müller, K.-J. Baeg, D.-Y. Kim, Y.-Y. Noh, Chem. Mat. 23 (2011) p. 341.
[24] G. Gelinck, Appl. Phys. Lett. 87 (2005) 092903.
[25] R. d. B. K.N.N. Unni, S. Dabos-Seignon, J.-M. Nunzi, Appl. Phys. Lett. 85 (2004) p. 1823.
[26] F. Ledoyen, P. Andry, A. Rambo, J. Lauzon, J. Appl. Phys. 72 (1992) 5756.
[27] G. Eberle, E. Bihler, W. Eisenmenger, Electr. Insul. Dielectr. Phenom., Ann. Rep. (1990) p. 41.
[28] G. Eberle, E. Bihler, W. Eisenmenger, IEEE Trans. Electron. Insul., IEEE 26 (1991) p. 69.
[29] G. Eberle, H. Schmidt, W. Eisenmenger, IEEE Trans. Dielectr. Electron. Insul. 3 (1996) 624.
[30] W. Eisenmenger, M. Haardt, Solid State Comm. 41 (1982) 917.
[31] W. Eisenmenger, H. Schmidt, B. Dehlen, Braz. J. Phys. 29 (1999) 295.
[32] M. Womes, E. Bihler, W. Eisenmenger, IEEE Trans. Electron. Insul. 24 (1989) 461.
[33] R. Kalbitz, P. Frübing, R. Gerhard, D. Taylor, Appl. Phys. Lett. 98 (2011) 033303.
[34] T.N. Ng, B. Russo, A.C. Arias, J. Appl. Phys. 106 (2009) 094504.
[35] F. Bauer, Ferroelectrics 49 (1983) 231.
[36] B. Dickens, E. Balizer, A. DeReggi, S. Roth, J. Appl. Phys. 72 (1992) 4258.
[37] R. Mehta, D. Silverman, J. Jacobs, J. Appl. Phys. 44 (1973) 3379.
[38] M. Wegener, Rev. Sci. Instrum. 79 (2008) 106103.
[39] H. Xu, J. Appl. Polym. Sci. 80 (2001) 2259.
[40] D.M. Taylor, N. Alves, J. Appl. Phys. 103 (2008) 054509.
[41] H. Sirringhaus, P. Brown, R. Friend, M. Nielsen, K. Bechgaard, B. Langeveld-Voss, A. Spieringand, R. Janssen, E. Meijer, P. Herwig, D. de Leeuw, Nature 401 (1999) 685.
[42] R. Kline, M. McGehee, M. Toney, Nat. Mater. 5 (2006) 222.
[43] Z. Bao, A. Dodabalapur, A. Lovinger, Appl. Phys. Lett. 69 (1996) 4108.

[44] A. Zen, J. Pflaum, S. Hirschmann, W. Zhuang, F. Jaiser, U. Asawapirom, J.P. Rabe, U. Scherf, D. Neher, Adv. Funct. Mater. 14 (2004) 757.
[45] A. Zen, M. Saphiannikova, D. Neher, J. Grenzer, S. Grigorian, U. Pietsch, U. Asawapirom, S. Janietz, U. Scherf, I. Lieberwirth, G. Wegner, Macromolecules 39 (2006) 2162.
[46] K. Asadi, P.W.M. Blom, D.M. de Leeuw, Appl. Phys. Lett. 99 (2011) 053306.
[47] L.-L. Chua, J. Zaumseil, J.-F. Chang, E.C.-W. Ou, P.K.-H. Ho, H. Sirringhaus, R.H. Friend, Nature 434 (2005) 194.
[48] G. Horowitz, M.E. Hajlaoui, R. Hajlaoui, J. Appl. Phys. 87 (2000) 4456.
[49] I. Guy, J. Unsworth, J. Appl. Phys. 61 (1987) 5374.
[50] N. Reynolds, K. Kim, C. Chang, S. Hsu, Macromolecules 22 (1989) 1092.
[51] G. Pfister, M. Abkowitz, R.G. Crystal, J. Appl. Phys. 44 (1973) 2064.
[52] H. Sussner, K. Dransfeld, J. Polym. Sci., Polym. Phys. Ed. 16 (1978) p. 529.
[53] E. Bihler, K. Holdik, W. Eisenmenger, IEEE Trans. Electron. Insul. 22 (1987) 207.
[54] E. Bihler, G. Neumann, G. Eberle, W. Eisenmenger, Electr. Insul. Dielectr. Phenom., Ann. Rep. (1990) p. 140.